Rejections Under 35 U.S.C. §112, First Paragraph

On pages 3-4 of the Office Action, the Examiner rejected claims 9-45 under 35 U.S.C. §112, first paragraph, for the reasons set forth therein. The Examiner has either repeated or modified his rejection under §112, first paragraph from the prior Office Action. Applicants maintain their arguments with respect to these claims, as found in the prior amendments filed November 21, 2000 and December 21, 2000.

Rejections Under 35 U.S.C. §112, Second Paragraph

On pages 4-7 of the Office Action, the Examiner rejected claims 9-45 under 35 U.S.C. §112, second paragraph for the reasons set forth therein. The Examiner has either repeated or modified his rejection under §112, second paragraph from the prior Office Action. Applicants maintain their arguments with respect to these claims, as found in the prior amendments filed November 21, 2000 and December 21, 2000.

Previous Prior Art Rejections Under 35 U.S.C. §§ 102 and 103

On pages 7-9, the Examiner rejected claims 9-45 under 35 U.S.C. §102(b) as being anticipated by Filseth (U.S. Patent No. 5,473,546).

On pages 9-11, the Examiner rejected claims 9-45 under 35 U.S.C. §103(a) as being unpatentable over Shinsha et al. (U.S. Patent No. 4,882,690); or Wang et al., "Restructuring Binary Decision Diagrams Based on Functional Equivalence," IEEE Design Automation, pp. 261-65; or Kuehlmann et al., "Equivalence Checking Using Cuts and Heaps," IEEE Proc. 1997 Design Auto. Conf., pp. 263-68.

The Examiner has either repeated or modified his prior art rejections from the prior Office Action. Applicants maintain their arguments with respect to these claims, as found in the prior amendments filed November 21, 2000 and December 21, 2000.

New Rejections Under 35 U.S.C. §102

On pages 11-13, the Examiner rejected claims 9-45 under 35 U.S.C. §102(b) as being anticipated by Yokomizo et al. ("A New Circuit Recognition and Reduction Method for Pattern Based Circuit Simulation," IEEE Custom Integrated Cir. Conf., pp. 9.4/1-9.4/4) or Chakrabarti et

al. ("An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-Circuits," IEEE Proc. Test Symp., pp. 237-243).

On pages 13-14, the Examiner rejected claims 9-45 under 35 U.S.C. §102(e) as being anticipated by Hachiya (U.S. Patent No. 6,031,979) or Fujisawa (U.S. Patent No. 5,809,284).

Applicants respectfully traverse these rejections for the reasons presented below.

Claim 9 of the present invention specifies that a plurality of partial circuits are extracted from a circuit to be simulated, and that the partial circuits exhibiting equivalent operational characteristics are integrated into one partial circuit (i.e., compressed) before the circuit is simulated. Independent claims 21, 33, and 45 recite similar language.

Yokomizo discloses a circuit recognition and reduction method for pattern-based circuit simulation. In Yokomizo, circuit elements extracted from layout pattern data are combined to reconstruct logic gates. Circuit data having a structure of the logic gates is recognized by the connection between gate terminals of the logic gates. The recognized circuit data is reduced by tracing signal flows and picking up the logic gates along specified critical paths. See Yokomizo at abstract. For each simulation of the specified critical paths, only subcircuit data corresponding to the critical paths are picked up from the entire circuit data to reduce the simulated circuit size (Yokomizo at p. 9.4.1). Most potential clocked transistors determined by an additional design rule (which requires that, for the entire circuit design, either the drain terminal of the clocked transistor must be connected to the output node of the gate, or that the source terminal of the clocked transistor must be connected to the power bus node) are successively eliminated (Yokomizo at p. 9.4.2).

Thus, the Yokomizo method involves circuit reconstruction, circuit recognition, and circuit reduction (by extracting subcircuits along critical paths and merging or eliminating parasitic elements), and not the circuit extraction, inspection for equivalent operational characteristics, and integration of equivalent circuits into one circuit of the present invention.

Chakrabarti discloses an improved hierarchical test pattern generating technique for combinational circuits with repetitive sub-circuits. In Chakrabarti, a plurality of identical gate-level sub-circuits are extracted from the combinational circuits and grouped together into high-level sub-circuits. Chakrabarti attempts to resolve incompatibility between the inputs and outputs of the high-level modules. In Chakrabarti, a hierarchical test pattern can be generated at high speed by using a circuit model having the high-level sub-circuits. See Chakrabarti at abstract. Unlike the present invention, Chakrabarti makes no mention of integrating partial

circuits, which are extracted from the circuit to be simulated, having equivalent operational characteristics into one partial circuit for circuit simulation.

Hachiya relates to a circuit partitioning apparatus used in parallel circuit simulation to uniformly partition a target circuit prior to the execution of circuit simulation (Hachiya at col. 1, lines 8-11). In Hachiya, an input target circuit is partitioned into clusters that are collected to create a plurality of sub-circuits. Simulation computation time is predicted for each sub-circuit by using a circuit matrix for each sub-circuit prior to the execution of parallel circuit simulation. Clustering is performed to create sub-circuits that require equal computation time for circuit simulation. See Hachiya at abstract.

Hachiya merges pairs of clusters. Before merging a candidate pair of clusters, the computation time prediction is used to determine the magnitude of a load after merging as the sum of the size of the two clusters. Merging is executed only if the computed value does not exceed a target magnitude. See Hachiya at col. 8, lines 62-67. Thus, Hachiya does not disclose integrating partial circuits that have equivalent operational characteristics into one circuit for circuit simulation.

Fujisawa relates to circuit simulation that is effective in transient analysis. In Fujisawa, an effective block extracting apparatus that determines whether each of a plurality of blocks in a circuit to be simulated includes nodes that have an influence on an accuracy of circuit simulation. Certain specified blocks, including these nodes, are extracted from all the blocks as effective blocks, and circuit simulation is performed only for these effective blocks. See Fujisawa at abstract. Thus, Fujisawa does not disclose integrating partial circuits that have equivalent operational characteristics into one circuit for circuit simulation.

As for the dependent claims, the dependent claims depend from the above-discussed independent claims and are patentable over the prior art for the reasons discussed above.

Therefore, Applicants submit that claims 9-45 patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under §§ 102 and 103.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding rejections have been overcome and/or rendered moot, and further, that all pending claims

patentably distinguish over the prior art. Thus, there being no further outstanding rejections, the application is submitted to be in condition for allowance, which action is earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on May 16, 2001

STASS & HALSEY

By: C. Joan Gilsdorf

Date: 5/16/01